WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate having a recess whose depth is not more than 6 nm;

a source region and a drain region which are formed in a surface region of the semiconductor substrate so as to sandwich the recess, each of the source region and the drain region being constituted of an extension region and a contact junction region;

a gate insulating film formed between the source region and the drain region in the semiconductor substrate; and

a gate electrode formed on the gate insulating film.

2. The semiconductor device according to claim 1, wherein a depth of the recess from a surface of the semiconductor substrate is deeper than the depth from the surface of the semiconductor substrate of an impurity concentration peak during ion implantation in the extension region.

3. The semiconductor device according to claim 1, wherein the extension regions are opposite to each other and extended toward a lower portion of the gate electrode, and a length of the extended portion is sufficiently shorter than two-third of the depth from the surface of the semiconductor substrate in the extension region.

4. The semiconductor device according to claim 1, wherein a material of the gate electrode is one of polysilicon, metal or its alloy, and a mixture of silicon and germanium.

5. The semiconductor device according to claim 1, wherein the gate electrode includes polysilicon formed on the gate insulating film and a silicide layer formed on this polysilicon layer, and the silicide layer is formed on the surfaces of the source region and the drain region.

6. A semiconductor device in which a plurality of MIS transistors comprising a semiconductor substrate, a source region and a drain region which are formed in a surface region of the semiconductor substrate, each of the source region and the drain region being constituted of an extension region and a contact junction region, a gate insulating film formed between the source region and the drain region in the semiconductor substrate, and a gate electrode formed on the gate insulating film are formed, and

the source region and the drain region of a part of said plurality of MIS transistors are formed so as to sandwich the recess which is formed in the semiconductor substrate and whose depth is not more than 6 nm.

7. The semiconductor device according to claim 6, wherein the MIS transistor having the source region and

the drain region, which are formed so as to sandwich the recess, is formed in a logic circuit.

8. The semiconductor device according to claim 6, wherein a depth of the recess from a surface of the semiconductor substrate is deeper than the depth from the surface of the semiconductor substrate of an impurity concentration peak during ion implantation in the extension region.

9. The semiconductor device according to claim 6, wherein the extension regions of the source region and the drain region, which are formed so as to sandwich the recess, are opposite to each other and extended toward a lower portion of the gate electrode, and a length of the extended portion is sufficiently shorter than two-third of the depth from the surface of the semiconductor substrate in the extension region.

10. The semiconductor device according to claim 6, wherein a material of the gate electrode is one of polysilicon, metal or its alloy, and a mixture of silicon and germanium.

11. The semiconductor device according to claim 6, wherein the gate electrode includes polysilicon formed on the gate insulating film and a silicide layer formed on this polysilicon layer, and the silicide layer is formed on the surfaces of the source region and the drain region.

12. A method of manufacturing a semiconductor

device, comprising:

forming a dummy gate insulating film on a semiconductor substrate, and forming a dummy gate electrode on the dummy gate insulating film;

carrying out ion implantation of an impurity into a surface region of the semiconductor substrate by using the dummy gate insulating film and the dummy gate electrode as a mask, and forming an extension region;

forming a gate sidewall insulating film on side faces of the dummy gate insulating film and the dummy gate electrode;

doping the impurity into a surface region of the semiconductor substrate by using the dummy gate insulating film, the dummy gate electrode and the gate sidewall insulating film as a mask to form a contact junction region, and forming a source region and a drain region which are constituted of the contact junction region and the extension region;

forming an interlayer insulating film on the semiconductor substrate so as to cover the dummy gate insulating film, the dummy gate electrode, and the gate sidewall insulating film;

polishing the interlayer insulating film until a surface of the dummy gate electrode is exposed, and planarizing the surface;

removing selectively the dummy gate insulating film and the dummy gate electrode to form a gate

opening region in the interlayer insulating film;

forming a recess on the surface region of the semiconductor substrate by oxidizing the surface of the semiconductor substrate which is exposed on a bottom portion of the gate opening region and by removing selectively the oxidized part;

insulating the surface of the recess in a bottom surface of the gate opening region to form a gate insulating film; and

burying a gate electrode material in the gate opening region to form a gate electrode.

13. The method according to claim 12, wherein a depth of the recess from a surface of the semiconductor substrate is deeper than the depth from the surface of the semiconductor substrate of an impurity concentration peak during ion implantation in the extension region.

14. The method according to claim 12, wherein the recess is formed by oxidizing the surface of the semiconductor substrate with plasma oxygen at a temperature not more than 600℃.

15. The method according to claim 12, wherein the depth of the recess is not more than 6 nm.

16. The method according to claim 12, wherein the gate insulating film is formed at least by adopting plasma oxidation.

17. The method according to claim 12, wherein

formation of the gate electrode comprises: burying polysilicon as the gate electrode material in the gate opening region; carrying out ion implantation of an impurity into the gate electrode material; and carrying out heat treatment at a temperature not lower than 1000℃ to activate the impurity.

18. The method according to claim 12, wherein a region where impurity concentration of the source/drain region is not lower than $1 \times 10^{19}/cm^3$ is not more than 10 nm from the surface of the semiconductor substrate.

19. The method according to claim 12, further comprising: burying polysilicon as the gate electrode material in the gate opening region, removing the interlayer insulating film, and forming a silicide layer on a surface of the gate electrode and the surface of the source/drain region.